REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed December 15, 2004. Claims 1 - 10 remain pending. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Information Disclosure Statement

Applicant acknowledges the Examiner's statement with respect to the U.S. patent references listed in the disclosure, and has filed an appropriate Information Disclosure Statement herewith. With the accompanying Information Disclosure Statement, these references should be made officially of record. Of course, it is presumed that they have been already considered, in connection with the Examiner's diligence in searching and examination of this application, and determined to be less relevant than the other references cited.

Rejections under 35 U.S.C. 102

The Office Action indicates that claim 1 stand rejected under 35 U.S.C. § 102(a,e) as being unpatentable over *Ni* (U.S. Patent No. 6,563,166). Applicant respectfully traverses the rejection.

With respect to *Ni*, that reference teaches a memory device includes a first memory cell and a second memory cell both controlled by a common control gate. Specifically, as shown in Figs. 2A, 2B, and 3C-3F and described in lines 32-37 of col. 4 of *Ni*, the spacers 130a and 130b each include a tunneling oxide layer 134a and 134b respectively disposed over the substrate 108 and functions as floating gate 136a and 136b of each of the flash memory cells 102a and 102b respectively.

Moreover, as described in lines 2-4 of col. 7 of *Ni*, the second conductive layer 130 functions as the floating gate. Thus, only one control gate 130a or 130b is formed on a sidewall of the select gate of a flash memory cell 102a or 102b. In other words, each of the flash memory cells 102a and 102b is disclosed as flash memory cell with single bit memory rather than a flash memory cell with dual-bit memory.

In addition, as shown in Figs. 2A, 2B, and 3E-3F and described in lines 53-57 of col. 4 of *Ni*, first and second outer spacers 148a and 148b are disposed adjacent the third dielectric layer 128a and 128b of the first and second stacks 110a and 110b and generally above the first and second drain regions 140a and 140b of the substrate 108. The first and second outer spacers 148a and 148b do not function as floating gates in the *Ni* reference. Thus, the control gate 106 of *Ni* overlies only one floating gate in a flash memory cell.

Turing now to the claims, claim 1 recites:

> 1. A dual-bit split gate flash memory comprising:
> a plurality of memory cells wherein ***each memory cell comprises***:
> a select gate overlying a substrate and isolated from said substrate by a select gate oxide layer;
> ***a first and second floating gate on opposite sidewalls of said select gate and isolated from said select gate by an oxide spacer***; and
> ***a control gate overlying said select gate and said first and second floating gates*** and isolated from said select gate and said first and second floating gates by a dielectric layers; and
> source and drain regions within said substrate and shared by adjacent said memory cells.

(*Emphasis Added*).

Applicant respectfully asserts that *Ni* is legally deficient for the purpose of anticipating claim 1. Specifically, Applicant respectfully asserts that *Ni* does not teach or otherwise disclose at least the features/limitations emphasized above in claim 1. Therefore, Applicant respectfully asserts that claim 1 is in condition for allowance.

Rejections under 35 U.S.C. 103

The Office Action indicates that claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Ni* in view of *Fulford*; that claims 3 and 4 are rejected over *Ni* in view of *Liang*; and that claims 5 - 10 are rejected over *Ni*. Applicant respectfully traverses the rejections.

In this regard, Applicant respectfully asserts that the cited secondary references do not teach or reasonably suggest the features/limitations emphasized above as lacking in the rejection of independent claim 1. Since claims 2 – 10 incorporate the features/limitations of claim 1, Applicant respectfully asserts that these claims also are in condition for allowance.

Cited Art of Record

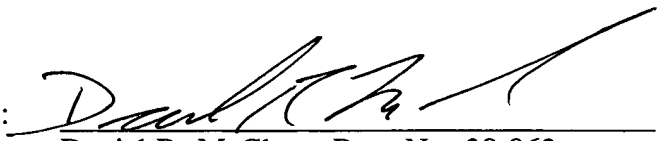
The cited art of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this Amendment and Response. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 
Daniel R. McClure, Reg. No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500